14. (Thrice Amended) A method for etching deep trenches in a substrate, comprising the steps of;

forming a hardmask on a silicon substrate of a wafer;

patterning the hardmask;

securing the wafer to an electrode in a plasma chamber;

maintaining the electrode at a temperature of between about 200 and about 450 degrees Celsius to achieve about the same temperature in the wafer; and

exposing the wafer to a reactive plasma to etch deep trenches into the silicon substrate of the wafer in accordance with the hardmask pattern, wherein the deep trenches have a depth of about 8um or greater and wherein the deep trench etching is performed for a ground rule design of 175nm or less.

23. (Thrice Amended) A method for etching deep trenches in a substrate, comprising the steps of:

clamping a wafer onto a electrode in a plasma chamber, the wafer comprising a silicon substrate;

maintaining the electrode at an elevated temperature between of about 200 degrees and 450 degrees Celsius;

exposing the wafer to a reactive plasma including Cl_2, BCL_3, Ar, O_2, and N_2;

applying a backside pressure to the clamped wafer using He to achieve thermal contact between the wafer and the electrode such that the wafer is maintained at about the same temperature as the electrode; and

applying a bias power to the wafer electrode to accelerate ions from the plasma to achieve etching of the silicon substrate to form deep trenches, wherein the deep trenches have a depth of about 8um or greater and wherein the deep trench etching is performed for a ground rule design of 175nm or less.